LPW

Practitioner's Docket No.: MST-013-1D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of (1st Inventor): Fu-Chieh Hsu

Assignee: Monolithic System Technology, Inc.

Serial No.: 10/676,695 Group No.: 2811

Filed: 9/30/2003 Examiner: Allan R. Wilson

For: "One-Transistor Floating-Body DRAM Cell In Bulk CMOS Process With Electrically Isolated Charge Storage Region"

Date: September 17, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

Sir:

In response to the outstanding Office Action dated August 30, 2004, in which the Examiner imposed a restriction requirement to election of invention for the above-referenced application, Applicant elects to prosecute the invention as in Group II, Claims 3-12 drawn to a method of making a semiconductor device, without traverse.

Applicant reserves the right to file divisional applications on the non-elected claims.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 17, 2004.

9-17-04 Carrie Reddick
Date Signature: Carrie Reddick